Government of India
The Semiconductor Integrated Circuits Layout Design Registry

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अनुक्रमणिका
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INTRODUCTION

The Semiconductor Integrated Circuits Layout-Design Registry has been made operational w.e.f. 1st May 2011 under the Semiconductor Integrated Circuits Layout-Design Act, 2000. In accordance with the provisions under the Act “The Semiconductor Integrated Circuits Layout-Design Journal” is required to be published. This Journal is being published on monthly basis on the 1st working day of the month. All the enquiries related to this Journal or any other information as required should be addressed to the Registrar, Semiconductor Integrated Circuits Layout-Design Registry. Any suggestions and comments are welcome.

(P. Ghatak)
REGISTRAR
A. Official Notes

The Registry is opened for public dealing from 10 am to 4 pm on all working days.

(P. Ghatak)
REGISTRAR
B. Jurisdiction of Office of the Semiconductor Integrated Circuits Layout Design Registry,

Vide Extraordinary Gazette Notification Part II-Section 3-Sub-section (ii) Published by authority No. 219 New Delhi, Monday, March 1, 2004 / Phalguna 11, 1925, the Semiconductor Integrated Circuits Layout-Design Registry (SICLDR) has its head office located in the Department of Information Technology, 6, CGO Complex, Lodhi Road, New Delhi. The territorial limits within which such office of the Semiconductor Integrated Circuits Layout-Design Registry may exercise its functions shall be the whole of India.

(P. Ghatak)
REGISTRAR
C. Applications advertised after acceptance – One.

Application Received for Registration under Semiconductor Integrated Circuits Layout Design Act 2000

Semiconductor Integrated Circuits Layout Design (SICLD) Registry has received an application for registration of 8 Port Microcontroller (BE 80501), Application no.1(1)/2013 in the name of M/s Bharat Electronics Ltd, Jalahalli, Bangalore, 560013, India. Details of the applications are as below:

1. **Date of Acceptance for registration of layout design:** 30/09/2014.
2. **Brief Description of the layout design:** The Layout has been made using 250 nm CMOS Standard cells, RAM cells and Embedded Flash memory for UMC, Taiwan foundry to meet the functionality of the circuitry. The layout has 21 mask tooling layers.
3. **Whether the layout design has been commercially exploited:** No
4. **The Address of the office of the registry where the application is filed:** SICLD Registry, DeitY

Anyone willing to oppose the filing of the application by M/s Bharat Electronics Ltd, Jalahalli, Bangalore, may kindly send their application to the SICLD Registry New Delhi.

A notice of opposition to the registration of a layout design under sub section (1) of section 11 shall be given in triplicate on Form LD-2 accompanied by prescribed fee within three months from the date of advertisement of the application for registration in the journal (www.sicldr.gov.in). The notice shall include a statement of the grounds on which the opponent objects to the registration.

To obtain details how to apply, please visit website: www.sicldr.gov.in

Duly filled Application Form may please be sent to:

**Registrar**

Semiconductor Integrated Circuits Layout Design Registry  
Department of Electronics and Information Technology  
Ministry of Communications and Information Technology (Government of India)  
Electronics Niketan, 6, CGO Complex,  
Lodhi Road, New Delhi: 110003
Schematic diagram of functional blocks
D. Notification of correction or amendment of application - Nil