The Semiconductor Integrated Circuits Layout Design Journal, June 2020

Government of India
The Semiconductor Integrated Circuits Layout Design Registry

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INTRODUCTION

The Semiconductor Integrated Circuits Layout-Design Registry has been made operational w.e.f. 1\textsuperscript{st} May 2011 under the Semiconductor Integrated Circuits Layout-Design Act, 2000. In accordance with the provisions under the Act “The Semiconductor Integrated Circuits Layout-Design Journal” is required to be published. This Journal is being published on the 2\textsuperscript{nd} working Friday of the month. All the enquiries related to this Journal or any other information as required should be addressed to the Registrar, Semiconductor Integrated Circuits Layout-Design Registry. Any suggestions and comments are welcome.

\textit{(O. P. Gupta)}

\textit{Registrar}
A. Official Notes

All the queries relating to registration of Semiconductor Integrated Circuits Layout Design may be obtained from the Registry between Timing 3:00 PM to 4.00 PM all working days.

(O. P. Gupta)
REGISTRAR
The Semiconductor Integrated Circuits Layout-Design Registry (SICLDR) has its head office located in the Boudhik Sampada Bhawan, Plot no. 32, Sector – 14, Dwarka, New Delhi-110075. The territorial limits within which such office of the Semiconductor Integrated Circuits Layout-Design Registry may exercise its functions shall be the whole of India.

(O. P. Gupta)
REGISTRAR
C. Applications advertised after acceptance – Nil

*no application received.
घ. आवेदन में शुष्क या संशोधन करने की अधिसूचना - शून्य

D. Notification of correction or amendment of application - Nil