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अर्द्धचालक एकीकृत परिपथ अभिन्यास डिजाइन जनरल जनवरी 2016

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INTRODUCTION

The Semiconductor Integrated Circuits Layout-Design Registry has been made operational w.e.f. 1\textsuperscript{st} May 2011 under the Semiconductor Integrated Circuits Layout-Design Act, 2000. In accordance with the provisions under the Act “The Semiconductor Integrated Circuits Layout-Design Journal” is required to be published. This Journal is being published on monthly basis on the 1\textsuperscript{st} working day of the month. All the enquiries related to this Journal or any other information as required should be addressed to the Registrar, Semiconductor Integrated Circuits Layout-Design Registry. Any suggestions and comments are welcome.

(P. Ghatak)

REGISTRAR
The Registry is opened for public dealing from 10 am to 4 pm on all working days.

(P. Ghatak)
REGISTRAR
B. Jurisdiction of Office of the Semiconductor Integrated Circuits Layout Design Registry,

As a result of Section 3(II) of the Extraordinary Gazette Notification dated March 1, 2004, the Semiconductor Integrated Circuits Layout Design Registry (SICLDR) is located in the Department of Information Technology, 6, CGO Complex, Lodhi Road, New Delhi. The territorial limits within which such office of the Semiconductor Integrated Circuits Layout-Design Registry may exercise its functions shall be the whole of India.

(P. Ghatak)
REGISTRAR
C. Applications advertised after acceptance – no application received.
D. Notification of correction or amendment of application - Nil