Government of India
The Semiconductor Integrated Circuits Layout Design Registry

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by Government of India, Office of the Registrar, Semiconductor Integrated Circuits Layout Design Registry,

Ministry of Communications and Information Technology
Department of Electronics & Information Technology

6, CGO Complex, Lodhi Road, New Delhi-110003.
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अनुक्रमणिका
INDEX

क. आधिकारिक टिप्पणियाँ
A. Official Notes

ख. अर्द्धचालक एकीकृत परिपथ अभिन्यास डिजाइन जजस्ट्री कायाधलय का अधिकार क्षेत्र
B. Jurisdiction of Office of the Semiconductor Integrated Circuits Layout Design Registry,

ग. स्वीकृति के पश्चात विज्ञापित आवेदन
C. Applications advertised after acceptance

घ. आवेदन में शुष्क या संशोधन करने की अधिसूचना
D. Notification of correction or amendment of application
INTRODUCTION

The Semiconductor Integrated Circuits Layout-Design Registry has been made operational w.e.f. 1st May 2011 under the Semiconductor Integrated Circuits Layout-Design Act, 2000. In accordance with the provisions under the Act “The Semiconductor Integrated Circuits Layout-Design Journal” is required to be published. This Journal is being published on monthly basis on the 1st working day of the month. All the enquiries related to this Journal or any other information as required should be addressed to the Registrar, Semiconductor Integrated Circuits Layout-Design Registry. Any suggestions and comments are welcome.

(P. Ghatak)
REGISTRAR
A. Official Notes

The Registry is opened for public dealing from 10 am to 4 pm on all working days.

(P. Ghatak)
REGISTRAR
B. Jurisdiction of Office of the Semiconductor Integrated Circuits Layout Design Registry,

Vide Extraordinary Gazette Notification Part II-Section 3-Sub-section (ii) Published by authority No. 219 New Delhi, Monday, March 1, 2004 / Phalguna 11, 1925, the Semiconductor Integrated Circuits Layout-Design Registry (SICLDR) has its head office located in the Department of Information Technology, 6, CGO Complex, Lodhi Road, New Delhi. The territorial limits within which such office of the Semiconductor Integrated Circuits Layout-Design Registry may exercise its functions shall be the whole of India.

(P. Ghatak)
REGISTRAR
C. Applications advertised after acceptance – One.

**Application Received for Registration under Semiconductor Integrated Circuits Layout Design Act 2000**

Semiconductor Integrated Circuits Layout Design (SICLD) Registry has received an application for registration of 50-60GHz sub harmonic IQ Mixer, Application no: 2(1)/2016 in the name of M/s Indian Space Research Organization Antariksh Bhavan, New BEL Road, Bangalore, 560231, India. Details of the applications are as below:

1. **Date of Receipt for registration of layout design**: 11/01/2016.
2. **Brief Description of the layout design**: The mixer IC function as an I-Q/Single Side Band Mixer working for both frequency up-conversion as well as down-conversion from 50-60 GHz. The Mixer is designed in Gallium Arsenide (GaAs) Monolithic Microwave Integrated Circuit (MMIC) Technology. Not requiring any DC supply, the Mixer is self biased and needs +10 dBm of LO input for optimum performance. Tested maximum conversion loss is 14 dB. Circuit size : 3.9*2.0*0.10 mm
3. **Whether the layout design has been commercially exploited**: No
4. **The Address of the office of the registry where the application is filed**: SICLD Registry, Electronics Niketan, 6 CGO Complex, Lodhi Road, New Delhi-110003.

Anyone willing to oppose the filing of the application by M/s Indian Space Research Organization Antariksh Bhavan, New BEL Road, Bangalore, may kindly send their application to the SICLD Registry Electronics Niketan, 6 CGO Complex, Lodhi Road, New Delhi-110003.

A notice of opposition to the registration of a layout design under sub section (1) of section 11 shall be given in triplicate on Form LD-2 accompanied by prescribed fee within three months from the date of advertisement of the application for registration in the journal (www.sicldr.gov.in). The notice shall include a statement of the grounds on which the opponent objects to the registration.

To obtain details how to apply, please visit website: [www.sicldr.gov.in](http://www.sicldr.gov.in)

Duly filled Application Form may please be sent to:

**Registrar**

Semiconductor Integrated Circuits Layout Design Registry  
Department of Electronics and Information Technology  
Ministry of Communications and Information Technology (Government of India)  
Electronics Niketan, 6, CGO Complex,  
Lodhi Road, New Delhi: 110003
50-60 GHz Sub-harmonic IQ Mixer

Functional Schematic:

IF1 (I)
DC-5 GHz

RF
50-60 GHz

Sub-Harmonic Mixer

LO Input
27.5 GHz, +10 dBm
(Typical)

IF2 (Q)
DC-5 GHz
The Layout Design:

- Input-Output PADS
- Resistor
- Transistor/Diodes
- Ground Via
- Metal Tracks / Microstriplines
D. Notification of correction or amendment of application - Nil