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INTRODUCTION

The Semiconductor Integrated Circuits Layout-Design Registry has been made operational w.e.f. 1st May 2011 under the Semiconductor Integrated Circuits Layout-Design Act, 2000. In accordance with the provisions under the Act “The Semiconductor Integrated Circuits Layout-Design Journal” is required to be published. This Journal is being published on monthly basis on the 1st working day of the month. All the enquiries related to this Journal or any other information as required should be addressed to the Registrar, Semiconductor Integrated Circuits Layout-Design Registry. Any suggestions and comments are welcome.

(SUNIL ALAG)

REGISTRAR, SEMICONDUCTOR INTEGRATED CIRCUITS LAYOUT-DESIGN REGISTRY
रजिस्ट्री आम जनता के लिए प्रातः 10.00 बजे से सांयः 4.00 बजे तक हर कार्य दिवस पर खुलेगी।

(सुनील अलग)
रजिस्ट्रार, अर्द्धचालक एकीकृत परिपथ अभियास डिजाइन रजिस्ट्री

The Registry is opened for public dealing from 10 am to 4 pm on all working days.

(SUNIL ALAG)
REGISTRAR, SEMICONDUCTOR INTEGRATED CIRCUITS LAYOUT-DESIGN REGISTRY
B. Jurisdiction of Office of the Semiconductor Integrated Circuits Layout Design Registry,

Vide Extraordinary Gazette Notification Part II-Section 3-Sub-section (ii) Published by authority No. 219 New Delhi, Monday, March 1, 2004 / Phalguna 11, 1925, the Semiconductor Integrated Circuits Layout-Design Registry (SICLDR) has its head office located in the Department of Information Technology, 6, CGO Complex, Lodhi Road, New Delhi. The territorial limits within which such office of the Semiconductor Integrated Circuits Layout-Design Registry may exercise its functions shall be the whole of India.

(SUNIL ALAG)
REGISTRAR, SEMICONDUCTOR INTEGRATED CIRCUITS LAYOUT-DESIGN REGISTRY
र. स्वीकृति के पश्चात विज्ञापित आवेदन – कोई आवेदन प्राप्त नहीं हुआ।
C. Applications advertised after acceptance – no application received.
D. Notification of correction or amendment of application - Nil