## The Semiconductor Integrated Circuits Layout Design Registry

**Government of India**

The Semiconductor Integrated Circuits Layout Design Registry

<table>
<thead>
<tr>
<th>Issue No.</th>
<th>Date</th>
<th>Issue Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>55/2015</td>
<td>18/12/2015</td>
<td>Friday</td>
</tr>
</tbody>
</table>

Published by Registrar, Semiconductor Integrated Circuits Layout Design Registry, New Delhi - 110003

Tel: 011-24364761, Fax: 011-24364788
अनुक्रमणिका

INDEX

क. आधिकारिक टिप्पणियां
   A. Official Notes

ख. अर्द्धचालक एकीकृत परिपथ अभिन्यास डिजाइन जजस्ट्री कार्यालय का अधिकार क्षेत्र
   B. Jurisdiction of Office of the Semiconductor Integrated Circuits Layout Design Registry,

ग. स्वीकृति के पश्चात विज्ञापित आवेदन
   C. Applications advertised after acceptance

घ. आवेदन में शुरुदि या संशोधन करने की अधिसूचना
   D. Notification of correction or amendment of application
INTRODUCTION

The Semiconductor Integrated Circuits Layout-Design Registry has been made operational w.e.f. 1st May 2011 under the Semiconductor Integrated Circuits Layout-Design Act, 2000. In accordance with the provisions under the Act “The Semiconductor Integrated Circuits Layout-Design Journal” is required to be published. This Journal is being published on monthly basis on the 1st working day of the month. All the enquiries related to this Journal or any other information as required should be addressed to the Registrar, Semiconductor Integrated Circuits Layout-Design Registry. Any suggestions and comments are welcome.

(P. Ghatak)
REGISTRAR
The Registry is opened for public dealing from 10 am to 4 pm on all working days.

(P. Ghatak)
REGISTRAR
B. Jurisdiction of Office of the Semiconductor Integrated Circuits Layout Design Registry,

Vide Extraordinary Gazette Notification Part II-Section 3-Sub-section (ii) Published by authority No. 219 New Delhi, Monday, March 1, 2004 / Phalguna 11, 1925, the Semiconductor Integrated Circuits Layout-Design Registry (SICLDR) has its head office located in the Department of Information Technology, 6, CGO Complex, Lodhi Road, New Delhi. The territorial limits within which such office of the Semiconductor Integrated Circuits Layout-Design Registry may exercise its functions shall be the whole of India.

(P. Ghatak)  
REGISTRAR
C. Applications advertised after acceptance – no application received.
D. Notification of correction or amendment of application - Nil