The Semiconductor Integrated Circuits Layout Design Journal December 2013

Government of India
The Semiconductor Integrated Circuits Layout Design Registry

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अनुक्रमणिका

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INTRODUCTION

The Semiconductor Integrated Circuits Layout-Design Registry has been made operational w.e.f. 1st May 2011 under the Semiconductor Integrated Circuits Layout-Design Act, 2000. In accordance with the provisions under the Act “The Semiconductor Integrated Circuits Layout-Design Journal” is required to be published. This Journal is being published on monthly basis on the 1st working day of the month. All the enquiries related to this Journal or any other information as required should be addressed to the Registrar, Semiconductor Integrated Circuits Layout-Design Registry. Any suggestions and comments are welcome.

(Yashvir Singh Tanwar)
Official Notes

i) The Registry is opened for public dealing from 10 am to 4 pm on all working days.

ii) All fees w.r.t Semiconductor Integrated Circuits Layout Design Registry may be accepted in ‘cash only’ till the notification for amendment of Rule 10(3)(4) is issued. This issues with the approval of competent authority.

(Yashvir Singh Tanwar)
REGISTRAR, SEMICONDUCTOR INTEGRATED CIRCUITS LAYOUT-DESIGN REGISTRY
Vide Extraordinary Gazette Notification Part II-Section 3-Sub-section (ii) Published by authority No. 219 New Delhi, Monday, March 1, 2004 / Phalgun 11, 1925, the Semiconductor Integrated Circuits Layout-Design Registry (SICLDR) has its head office located in the Department of Information Technology, 6, CGO Complex, Lodhi Road, New Delhi. The territorial limits within which such office of the Semiconductor Integrated Circuits Layout-Design Registry may exercise its functions shall be the whole of India.

(Yashvir Singh Tanwar)

REGISTRAR, SEMICONDUCTOR INTEGRATED CIRCUITS LAYOUT-DESIGN REGISTRY
C. Applications advertised after acceptance —
No application received from 1st November to 30th November 2013.
D. Notification of correction or amendment of application - Nil